

What is claimed is:

1. A semiconductor memory device, comprising:

a cell array including bit lines arranged at a uniform pitch; and

5 a plurality of bit line selection transistors connected to respective bit line ends for selectively connecting said bit line to a sense amp, wherein said bit line selection transistors are translationally arrayed in a direction perpendicular to said bit line at an average 10 array pitch greater than eight times said pitch of said bit lines.

2. The semiconductor memory device according to

claim 1, wherein said average array pitch is related to an 15 integer other than said bit line pitch multiplied by a power of 2.

3. The semiconductor memory device according to

claim 1, wherein said bit line selection transistors are 20 arrayed in said direction perpendicular to said bit line at two or more different array pitches.

4. The semiconductor memory device according to

claim 1, wherein said bit line selection transistors are 25 arrayed on a plurality of stages in the longitudinal direction of said bit line, having two or more different array stages corresponding to positions of said bit lines.

5. The semiconductor memory device according to  
claim 1, wherein said bit line selection transistors are  
laid out to have a gate width direction orthogonal to said  
5 bit line.

6. The semiconductor memory device according to  
claim 1, wherein said bit line selection transistors are  
laid out to have a gate length direction orthogonal to said  
10 bit line.

7. The semiconductor memory device according to  
claim 1, wherein a bit line selection transistor for  
selecting an even bit line and a bit line selection  
15 transistor for selecting an odd bit line adjacent thereto  
are formed to share a common source/drain diffusion layer,  
said common source/drain diffusion layer being connected to  
a sensing bit line that leads to a sense amp shared by said  
even bit line and said adjacent odd bit line.

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8. The semiconductor memory device according to  
claim 1, wherein said cell array includes electrically  
erasable programmable non-volatile semiconductor memory  
cells arrayed.

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9. The semiconductor memory device according to  
claim 8, wherein said non-volatile semiconductor memory

cells configure a NAND cell unit including a plurality of serially connected cells, each pair of adjacent cells sharing a source/drain diffusion layer.

5           10. An electronic card including said semiconductor memory device according to claim 9 mounted thereon.

11. An electronic device, comprising:

a card interface;

10           a card slot connected to said card interface; and  
              said electronic card according to claim 10  
              electrically connectable to said card slot.

12. The electronic device according to claim 11,  
15        wherein said electronic device comprises a digital camera.

13. A semiconductor memory device, comprising:

a cell array including bit lines arranged at a

uniform pitch; and

20           a plurality of bit line selection transistors  
              connected to respective bit line ends for selectively  
              connecting said bit line to a sense amp, wherein said bit  
              line selection transistors are translationally arrayed in a  
              direction perpendicular to said bit line at an average  
25        array pitch deviated from an integer multiple of said pitch  
              of said bit lines.

14. The semiconductor memory device according to  
claim 13, wherein said bit line selection transistors are  
arrayed in said direction perpendicular to said bit line at  
two or more different array pitches.

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15. The semiconductor memory device according to  
claim 13, wherein said bit line selection transistors are  
arrayed on a plurality of stages in the longitudinal  
direction of said bit line, having two or more different  
10 array stages corresponding to positions of said bit lines.

16. The semiconductor memory device according to  
claim 13, wherein said bit line selection transistors are  
laid out to have a gate width direction orthogonal to said  
15 bit line.

17. The semiconductor memory device according to  
claim 13, wherein said bit line selection transistors are  
laid out to have a gate length direction orthogonal to said  
20 bit line.

18. The semiconductor memory device according to  
claim 13, wherein a bit line selection transistor for  
selecting an even bit line and a bit line selection  
25 transistor for selecting an odd bit line adjacent thereto  
are formed to share a common source/drain diffusion layer,  
said common source/drain diffusion layer being connected to

a sensing bit line that leads to a sense amp shared by said even bit line and said adjacent odd bit line.

19. The semiconductor memory device according to  
5 claim 13, wherein said cell array includes electrically  
erasable programmable non-volatile semiconductor memory  
cells arrayed.

20. The semiconductor memory device according to  
10 claim 19, wherein said non-volatile semiconductor memory  
cells configure a NAND cell unit including a plurality of  
serially connected cells, each pair of adjacent cells  
sharing a source/drain diffusion layer.

15 21. An electronic card including said semiconductor  
memory device according to claim 20 mounted thereon.

22. An electronic device, comprising:  
a card interface;  
20 a card slot connected to said card interface; and  
said electronic card according to claim 21  
electrically connectable to said card slot.

23. The electronic device according to claim 22,  
25 wherein said electronic device comprises a digital camera.